1. An apparatus for programmatically detecting time-gap defects in a computer system having devices interconnected to one another, the apparatus comprising:

a memory device configured to store data structures comprising executables and operational data;

a processor operably connected to the memory device to process the data structures;

a controller configured to control an exchange of data between the devices; and

the memory device, wherein the data structures further comprise a detection module, executable by the processor and comprising:

an operation module configured to initiate an exchange of data between at least two of the devices;

an interrupt module configured to interrupt the exchange of data and insert a delay time having a programmable value; and

a verification module configured to determine whether an error occurred in the exchange and remained undetected to the computer system.

2. The apparatus of claim 1, wherein the detection module further comprises an input module configured to receive operating parameters from a user.

3. The apparatus of claim 2, wherein the detection module further comprises an initialization module configured to initialize variables, internal to the detection module, with the operating parameters.

4. The apparatus of claim 3, wherein the operating parameters are selected from the group consisting of a maximum delay time value, a delay step value, a minimum delay step value, and an initial delay time value.

5. The apparatus of claim 4, wherein the interrupt module randomly interrupts the exchange of data.

6. The apparatus of claim 5, wherein the verification module is further configured to increment the delay time value by the delay step value and retest an exchange of data by the controller until an error is detected.

7. The apparatus of claim 6, wherein the verification module if further configured to decrease the delay step value and retest an exchange of data by the controller when an error is detected.

8. The apparatus of claim 7, wherein the delay step value is decreased until the minimum delay step value is reached.

9. The apparatus of claim 8, wherein the detection module is iterated by the processor a sufficient number of times to create a statistical sample significant to a user.

10. An article including a computer readable medium configured to store data structures comprising executables and operational data, the data structures comprising:

a controller driver configured to facilitate exchanging of data between devices in a computer system, and to detect errors occurring in the exchanging process;

a detection module, executable to detect errors occurring in, yet undetected by the computer system, due to timing inconsistencies between the devices, the detection module comprising:

an operation module configured to initiate an exchange of data between at least two of the devices;

an interrupt module configured to interrupt the exchange of data and insert a delay time having a programmable value; and

a verification module configured to determine whether an error occurred in the exchange and remained undetected to the computer system.

11. The article of claim 1, wherein the verification module is further configured to detect a discrepancy between a first device and a second device in selection of a timing increment relied upon.

12. A method for programmatically detecting time-gap defects in computer system components, the method comprising:

providing a detection module configured to execute on a processor to initiate, detect, and verify reporting of errors in data exchanges and operations, controlled by controllers, between devices in a computer system, yet remaining undetected to the computer system.

loading the detection module onto a computer system comprising a processor, a memory, devices connected to exchange data with one another, and controllers for controlling the exchange of data therebetween; and

executing the detection module by the processor.

13. The method of claim 12, wherein executing the detection module further comprises:

effectuating an exchange of data between devices in a computer system;

interrupting the exchange of data by inserting a delay time therein;

checking the data for any errors incurred by the delay time; and

identifying devices incurring errors without detection thereof.

14. The apparatus of claim 13, wherein executing the detection module further comprises reporting, to a user, any errors undetected in the exchange.

15. The method of claim 14, wherein executing the detection module further comprises incrementing the delay time by a delay step value and re-executing the exchange until an error is incurred.

16. The method of claim 15, where the detection module is configured to prevent the delay time from exceeding a maximum delay time.

17. The method of claim 16, wherein executing the detection module further comprises decrementing the delay step value, when an error is incurred, and re-executing the exchange until a minimum delay step value is reached.

18. The method of claim 17, further comprising requesting, from a user, initial values for operating parameters of the detection module, wherein the operating parameters are selected from the group consisting of the maximum delay time, the delay step value, the minimum delay step value, and an initial delay time.

19. The method of claim 18, further comprising setting an "in process" flag when the exchange begins and resetting the "in process" flag when the exchange ends.

20. The method of claim 19, further comprising re-executing the detection module a sufficient number of times to create a statistical sample significant to a user.